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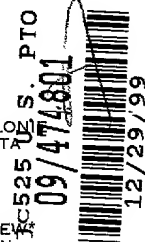
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## BOX PATENT APPLICATION

Assistant Commissioner for Patents  
 Washington, DC 20231

Sir:

Transmitted herewith for filing is the patent application of

Inventor(s): Kaoru ADACHI

For: IMAGE DISPLAY APPARATUS FOR PHOTOGRAPHING AN OBJECT AND  
 DISPLAYING THE PHOTOGRAPHED IMAGE

Enclosed are:

- ☒ A specification consisting of twenty-two (22) pages
- ☒ Five (5) sheet(s) formal drawings
- ☒ An assignment of the invention
- ☒ Certified copy of Priority Document(s)
- ☒ Executed Declaration (☒ Original ☐ Photocopy)
- ☐ A statement (☐ original ☐ photocopy) to establish small entity status under 37 C.F.R. § 1.9 and 37 C.F.R. § 1.27
- ☐ Preliminary Amendment
- ☒ Information Disclosure Statement, PTO-1449 and reference(s)
- ☐ Other:

The filing fee has been calculated as shown below:

			LARGE ENTITY	SMALL ENTITY
BASIC FEE			\$690.00	\$345.00
	NUMBER FILED	NUMBER EXTRA	RATE FEE	RATE FEE
<b>TOTAL CLAIMS</b>	11- 20 =	0	X 18 = \$0.00	x 9 = \$0.00
<b>INDEPENDENT CLAIMS</b>	4- 3 =	1	x 78 = \$78.00	x 39 = \$0.00
<input type="checkbox"/> MULTIPLE DEPENDENT CLAIMS PRESENTED			+ \$260.00	+ \$130.00
<b>TOTAL</b>			\$768.00	\$0.00

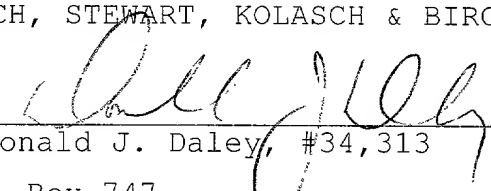
- ☒ A check in the amount of \$808.00 to cover the filing fee and recording fee (if applicable) is enclosed.
- ☐ Please charge Deposit Account No. 02-2448 in the amount of \$0.00. A triplicate copy of this transmittal form is enclosed.
- ☒ Please send correspondence to:  
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Respectfully submitted,

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 Attachments

1           IMAGE DISPLAY APPARATUS FOR PHOTOGRAPHING AN OBJECT  
                  AND DISPLAYING THE PHOTOGRAPHED IMAGE

BACKGROUND OF THE INVENTION

5           Field of the Invention

          The present invention relates to an image display apparatus for photographing an object by imaging devices and displaying the photographed image by a liquid crystal display and the like.

10

Description of the Background Art

          In image display apparatus such as a video camera and a digital still camera, an image of an object is converted to an image signal by imaging devices, and the image signal undergoes an image processing to be displayed by a liquid crystal display and the like. FIG. 6 shows an example of a conventional image display apparatus. In FIG. 6, an imaging section 60 comprises, for example, CCD (Charge Coupled Device) imaging devices, converts an image of an object to an image signal and outputs the image signal to a signal conversion section 62. A white balance circuit 64 in the signal conversion section 62 adjusts the white balance of the image signal in response to a color temperature change. A gamma correction circuit 66 performs a processing to give a non-linearity to the image signal.

          Furthermore, in the case where the CCD imaging devices included in the imaging section 60 are color imaging devices having a color filter adopting the Bayer array or a G-stripe RB checkers array, an R-signal, a B-signal and a G-signal cannot be obtained

1 simultaneously by the CCD imaging devices, so that if  
any processing is not performed, the image is displayed  
to be in a mosaic state. Accordingly, an interpolation  
processing circuit 68 in the signal conversion section  
5 62 interpolates lacks of any of the R, B and G-signals  
by its interpolation processing.

When the pixels of the CCD imaging devices  
included either in a horizontal direction or in a  
10 vertical direction are different in number from those of  
a display section 76, an interpolation processing  
circuit 68 performs a thinning processing or an  
interpolation processing suitably using a memory circuit  
70, whereby the number of pixels output from the CCD  
15 imaging devices is converted to be equal to that of the  
display section 76.

A gray scale correction circuit 72 in the  
signal conversion section 62 executes a gray scale  
20 correction such as a dither processing so that an image  
originated from the image signal processed looks better  
when it is displayed by the display section 76. A gamma  
correction circuit 74 performs a gamma correction for  
the image signal processed by the gray scale correction  
25 circuit 72 to output it to the display section 76. The  
display section 76 comprises, for example, an LCD  
(Liquid Crystal Display), and displays the image based  
on the image signal processed by the signal conversion  
section 62.

30

In the CCD imaging devices included in the  
imaging section 60, since signals generated by a large  
number of photodiodes, which are arranged

1 two-dimensionally in the form of a matrix, are serially  
 output on a pixel-by-pixel basis, the signal conversion  
 section 62 has been obliged to process the signals  
 serially. Since the refresh rate of the display section  
 5 76 is generally 60 Hz, the signal conversion section 62  
 had to process all signals of the pixels of one field,  
 which are output from the CCD imaging devices, within a  
 period of 1/60 seconds.

10 Although power consumption can be reduced by  
 lowering a clock frequency in performing a digital  
 signal processing, in the case of the image display  
 apparatus, there is a certain limitation in reducing the  
 clock frequency because the refresh rate of the display  
 15 section 76 is generally not changeable, and it is  
 difficult for the image display apparatus to be designed  
 in reduced power consumption.

Furthermore, since a quantity of signals to  
 20 be processed in the signal conversion section 62 becomes  
 larger with an increase in number of the pixels of the  
 CCD imaging devices, a high speed processing is required  
 for the image display apparatus in order to process  
 these signals within a certain period (1/60 seconds),  
 25 and the clock frequency becomes higher, resulting in  
 more increase in power consumption.

#### SUMMARY OF THE INVENTION

It is therefore an object of the present  
 30 invention to provide an image display apparatus which  
 is free from the drawbacks of the foregoing prior art,  
 and improved in power consumption by performing a  
 signal processing at a low speed.

1           To accomplish the foregoing subjects, an image  
display apparatus of the present invention comprises:  
imaging section having photoelectric conversion devices  
arranged in the form of a matrix, the imaging section  
5 sequentially outputting signals generated by the  
photoelectric conversion devices in parallel column by  
column of the matrix; and display section having display  
devices arranged in the form of a matrix, which displays  
an image represented by the signals applied thereto at  
10 the time of application of driving pulses, the display  
section applying the signals output in parallel from the  
imaging section to these display devices column by  
column and supplying the driving pulses line by line in  
a predetermined order.

15           Furthermore, an image display apparatus of the  
present invention comprises: imaging section having  
photoelectric conversion devices arranged in the form of  
a matrix, the imaging section sequentially outputting  
20 signals generated by the photoelectric conversion  
devices in parallel column by column of the matrix;  
signal conversion section for performing a processing  
for the signals output from the imaging section in  
parallel column by column and outputting the processed  
25 signals in parallel; and display section having display  
devices arranged in the form of a matrix, which display  
an image represented by signals applied thereto at the  
time of application of driving pulses, the display  
section applying the signals output in parallel from the  
30 signal conversion section to these display devices  
column by column and supplying the driving pulses line  
by line in a predetermined order.

1           Here, the image display apparatus may  
advantageously comprises a parallel-to-serial conversion  
section for converting the signals output in parallel  
from the signal conversion section to serial signals.

5           Furthermore, an image display apparatus of the  
present invention comprises: imaging section having  
photoelectric conversion devices arranged in the form of  
a matrix, the imaging section sequentially outputting  
10 signals generated by the photoelectric conversion  
devices in parallel column by column of the matrix;  
signal conversion section for performing a processing  
for the signals output in parallel from the imaging  
section column by column and outputting the processed  
15 signals in parallel; and parallel-to-serial conversion  
section for converting the signals output in parallel  
from the signal conversion section to serial signals.

20           Still furthermore, an image display apparatus  
of the present invention comprises: serial-to-parallel  
conversion section for converting signals serially input  
thereto to parallel signals and outputting the signals;  
and display section having display devices arranged in  
the form of a matrix, which display an image represented  
25 by signals applied thereto at the time of application of  
driving pulses, the display section applying the signals  
output in parallel from the serial-to-parallel  
conversion section to these display devices column by  
column and supplying the driving pulses row by row in a  
30 predetermined order.

#### BRIEF DESCRIPTION OF THE DRAWINGS

1           The objects and features of the present invention will become more apparent from consideration of the following detailed description taken in conjunction with the accompanying drawings in which:

5           FIG. 1 is a schematic block diagram showing an embodiment of an image display apparatus in accordance with the present invention;

          FIG. 2 is a drawing showing a constitution of an example of a conventional CCD;

10          FIG. 3 schematically shows an example of the constitution of a conventional LCD;

          FIG. 4 is a schematic block diagram showing an alternative embodiment of an image display apparatus in accordance with the present invention;

15          FIG. 5 is a schematic block diagram showing an example of a display apparatus in accordance with the present invention; and

          FIG. 6 is a schematic block diagram showing an example of a conventional image display apparatus.

#### 20          DESCRIPTION OF THE PREFERRED EMBODIMENTS

          In FIG. 1, the image display apparatus converts an image of an object to an image signal by an imaging section 10, and performs a processing for the image signal by a signal conversion section 20, thus displaying an image by a display section 30. The image display apparatus can widely be applied to a video camera, a digital still camera and the like.

30          The imaging section 10 is, for example, an interline CCD. The imaging section 10 has a large number of photodiodes 12 arranged in an imaging region in the form of a matrix (M lines × N columns or



1 pixels) and vertical transfer paths 14-1 to 14-N  
arranged adjacent to the respective lines of the  
photodiodes 12. Each of the photodiodes 12 is connected  
to corresponding one of the vertical transfer paths 14-1  
5 to 14-N via transfer gates (not shown), and each lower  
end of the vertical transfer paths 14-1 to 14-N is  
connected to corresponding one of output circuits 16-1  
to 16-N.

10 Each of the photodiodes 12 converts the image  
of the object, which is focussed on its surface, to a  
signal charge pixel by pixel by a photoelectric  
conversion and stores it therein. Field shift pulses  
are alternately supplied to the transfer gates arranged  
15 in the odd-numbered lines and the transfer gates  
arranged in the even-numbered lines every field during  
a vertical blanking period. When the field shift pulses  
are supplied to the transfer gates, the signal charge  
stored in the photodiodes 12 moves to the vertical  
20 transfer paths 14-1 to 14-N through the transfer gates.

Vertical driving pulses are supplied to the  
vertical transfer paths 14-1 to 14-N during a horizontal  
blanking period. The signal charge in the vertical  
25 transfer paths 14-1 to 14-N is transferred toward output  
circuits 16-1 to 16-N in response to the vertical  
driving pulses. Every time a vertical driving pulse is  
supplied, each of the signal charge in the vertical  
transfer paths 14-1 to 14-N is moved toward  
30 corresponding one of the output circuits 16-1 to 16-N  
line by line, and sequentially arrives at corresponding  
one of the output circuits 16-1 to 16-N within one field  
period. The output circuits 16-1 to 16-N serially

1 convert each of the signal charge arriving from the  
vertical transfer paths 14-1 to 14-N to a signal  
voltage, and output signals 200-1 to 200-N,  
respectively.

5

As described above, in this embodiment, the  
signal charge generated by the photodiodes 12 is  
transferred to the output circuits 16-1 to 16-N on the  
vertical transfer paths 14-1 to 14-N, and converted to  
10 the signal voltage by the output circuits 16-1 to 16-N  
path by path. Each of the output circuits 16-1 to 16-N  
outputs the signal voltage by one pixel per horizontal  
scanning period. That is, the signal voltage equivalent  
to N pixels (equivalent to one line) is output from the  
15 N output circuits in parallel.

FIG. 2 shows an example of a conventional  
CCD, which is illustrated for comparing it with the CCD  
of this embodiment. The conventional CCD comprises the  
20 photodiodes 12, the vertical transfer paths 14-1 to  
14-N, a horizontal transfer path 50 and output circuit  
52. The conventional CCD is different from the CCD in  
the imaging section 10 of FIG. 1 in that the lower ends  
of the vertical transfer paths 14-1 to 14-N are  
25 connected to a horizontal transfer path 50 and the left  
end of the horizontal transfer path 50 is connected to  
an output circuit 52.

In FIG. 2, the vertical driving pulses are  
30 supplied to the vertical transfer paths 14-1 to 14-N,  
and the horizontal driving pulses are supplied to the  
horizontal transfer path 50. The signal charge moved to  
the vertical transfer paths 14-1 to 14-N during the

1 vertical blanking period is transferred toward the  
horizontal transfer path 50 line by line in response to  
the vertical driving pulses supplied during the  
horizontal blanking period. The signal charge arrived  
5 at the lower ends of the vertical transfer paths 14-1 to  
14-N moves to the horizontal transfer path 50  
sequentially.

10 In the above-described manner, every time the  
vertical driving pulses are supplied to the vertical  
transfer paths 14-1 to 14-N, the signal charge  
equivalent to one pixel is moved from each of the  
vertical transfer paths 14-1 to 14-N to the horizontal  
transfer path 50, that is, the signal charge equivalent  
15 to N pixels (equivalent to one line) is moved from the N  
vertical transfer paths 14-1 to 14-N to the horizontal  
transfer path 50 in parallel.

20 The horizontal transfer path 50 transfers the  
signal charge, which was moved from the vertical  
transfer paths 14-1 to 14-N, toward the output circuit  
52 in response to the horizontal driving pulses  
repeatedly supplied during the horizontal scanning  
period. The signal charges equivalent to one line,  
25 which were moved to the horizontal transfer 50,  
sequentially arrive at the output circuit 52 within one  
horizontal scanning period. The output circuit 52  
converts the arrived signal charge to a signal voltage  
and outputs the signal voltage.

30

As described above, in the conventional CCD  
of FIG. 2, the signal charge, which has been  
photoelectrically converted by the photodiodes 12

1 arranged in the form of a matrix, is transferred by the  
vertical transfer paths 14-1 to 14-N, and moved to the  
horizontal transfer path 50. The signal charge is  
transferred from the horizontal transfer path 50 to the  
5 output circuit 52, and the signal voltage corresponding  
to the N pixels is serially output from the output  
circuit 52 every horizontal scanning period.

Contrary to this, in the imaging section 10  
10 according to this embodiment of FIG. 1, the signal  
charge transferred by the vertical transfer paths 14-1  
to 14-N is transferred to the output circuits 16-1 to  
16-N connected to the respective vertical transfer paths  
14-1 to 14-N, and the signal voltage equivalent to one  
15 pixel is output from each of the output circuits 16-1 to  
16-N every horizontal scanning period. The N signal  
voltages equivalent to N pixels are output from the N  
output circuits in parallel every horizontal scanning  
period.

20 Accordingly, in the imaging section 10 of this  
embodiment, since the imaging section 10 does not have  
the horizontal transfer path 50 provided in the  
conventional CCD, the horizontal driving pulse to be  
25 supplied to the horizontal transfer path is unnecessary,  
so that power consumption can be more reduced. Although  
the CCD is employed for the imaging section 10 in this  
embodiment, other types of imaging device such as a MOS  
(Metal Oxide Semiconductor) imaging device may be  
30 employed.

The signal conversion section 20 is connected  
to the imaging section 10 of FIG. 1. The signal



1 display section 30 in the horizontal direction is  
different from that of the imaging section 10, since  
the signal conversion section 20 performs a signal  
processing so that the number of outputs of the section  
5 20 becomes equal to the number of pixels of the display  
in the horizontal direction, the number of outputs of  
the section 20 varies in accordance with the number of  
pixels of the display section 30 in the horizontal  
direction.

10

The display section 30 is connected to the  
signal conversion section 20. This display section 30  
is, for example, a liquid crystal display (LCD), and has  
a structure that a plurality of display devices composed  
15 of field effect transistors 34 and liquid crystal  
devices 36 are arranged in the form of a matrix (M lines  
× N columns). Each of the field effect transistors 34  
operates as a switch, and allows its source and drain to  
be conductive with each other when a voltage is applied  
20 to its gate. Each of the liquid crystal devices 36 is  
connected to the source of corresponding one of the  
field effect transistors 34, and stores charge in  
response to the voltage applied to the drain of the  
field effect transistor 34 when this transistor 34 is  
25 made to be in a conduction state.

The gate of each of the field effect  
transistors 34 is connected to corresponding one of gate  
buses 40-1 to 40-M line by line, and one end of each of  
30 the gate buses is connected to a vertical driving  
circuit 38. The drain of each of the field effect  
transistors 34 is connected to corresponding one of  
drain buses 42-1 to 42-N column by column, and one end

1 of each of the drain buses 42-1 to 42-N is connected to  
an output port of corresponding one of input circuits  
32-1 to 32-N. Input ports of the input circuits 32-1 to  
32-N are connected to respective output terminals of the  
5 signal conversion section 20. The input circuits 32-1  
to 32-N receive signals 202-1 to 202-N output from the  
signal conversion section 20, respectively, and output  
predetermined voltage to the drain buses 42-1 to 42-N,  
respectively.

10

When the vertical driving circuit 38  
refreshes, for example, an image display every field,  
the vertical driving circuit 38 alternately scans the  
gate buses arranged in the odd-numbered lines and the  
15 gate buses arranged in the even-numbered lines every  
field period sequentially in response to the horizontal  
synchronous signal, and outputs a gate driving pulse to  
the gate bus scanned.

20 When the gate driving pulse is supplied to the  
gate bus 40 connected to the gate of the field effect  
transistor 34, the drain and source of the field effect  
transistor 34 are made conductive. On the other hand,  
the signals 202-1 to 202-N are input to the input  
25 circuits 32-1 to 32-N from the signal conversion  
section 20 in synchronization with the gate driving  
pulse, and the input circuits 32-1 to 32-N supply  
voltage corresponding to the signals to the drain buses  
42-1 to 42-N, respectively.

30

For example, when the gate driving pulse is  
supplied to the gate bus 40-1 from the vertical driving  
circuit 38 and voltage corresponding to the signals

1 202-1 to 202-N is supplied from the input circuits 32-1  
to 32-N to the drain buses 42-1 to 42-N, the field  
effect transistors 34 connected to the gate bus 40-1 are  
made to be in their conduction state, and charge  
5 associated with the magnitudes of the voltage applied to  
the drains of the field effect transistors 34 is stored  
in the liquid crystal devices 36.

10 The vertical driving circuit 38 scans all of  
the gate buses 40-1 to 40-M within two-field period in  
a predetermined order in response to the horizontal  
synchronous signal, and supplies the gate driving  
voltage to the gate bus scanned. The input circuits  
32-1 to 32-N output the voltage, which corresponds to  
15 the signals 202-1 to 202-N from the signal conversion  
section 20, to the drain buses 42-1 to 42-N in  
synchronization with the horizontal synchronous signal.

20 Accordingly, the charge corresponding to the  
magnitudes of the signals 202-1 to 202-N is stored in  
the liquid crystal devices 36 arranged in the form of  
a matrix, and held therein. Immediately after the  
charge is stored in the liquid crystal device 36, the  
state of the liquid crystal forming the liquid crystal  
25 device 36 changes in response to the quantity of the  
charge, the liquid crystal device 36 allows light guided  
from the back light disposed behind the device 36 to be  
shield or passed therethrough in response to the  
quantity of the charge stored.

30

Thus, an image represented by the signals  
202-1 to 202-N, which are output from the signal  
conversion section 20, is displayed by the display



1 section 30. The charge stored in the liquid crystal  
device 36 is updated every two fields in this  
embodiment. Although the LCD is used for the display  
section 30 of this embodiment, a display using an LED  
5 (Light Emitting Diode) as a display device may be  
employed.

FIG. 3 shows an example of a conventional  
LCD, which is illustrated for being compared with the  
10 LCD of this embodiment. Although this conventional LCD  
is the same as the display section 30 of FIG. 1 in  
constitution of the field effect transistors 34, the  
liquid crystal devices 36 and the vertical driving  
circuit 38 and in connection as to the gate buses 40-1  
15 to 40-N and the drain buses 42-1 to 42-N, the  
conventional LCD differs from the display section 30 of  
FIG. 1 in that a horizontal register circuit 54 is  
provided instead of the input circuits 32-1 to 32-N and  
one end of each of the drain buses 42-1 to 42-N is  
20 connected to the horizontal register circuit 54.

In FIG. 3, the horizontal register circuit 54  
is adapted to hold temporarily a signal equivalent to  
one line for the number N of pixels. The horizontal  
25 register circuit 54 sequentially receives a signal input  
thereto serially from the outside in response to clock  
signals, and sequentially shifts it. Then, when the  
horizontal register circuit 54 holds signals equivalent  
to one line, the horizontal register circuit 54 outputs  
30 the voltage corresponding to the signals held therein to  
the drain buses 42-1 to 42-N. The horizontal register  
circuit 54 executes such processing iteratively in timed  
with a horizontal synchronous signal, and outputs

1 voltage corresponding to the signals 202-1 to 202-N, in  
synchronous with gate driving pulses which are output  
from the vertical driving circuit 38 to the drain buses  
42-1 to 42-N.

5

As described above, in the conventional LCD of  
FIG. 3, the horizontal register circuit 54 is provided,  
which converts the signals serially input thereto line  
by line to the voltage corresponding to the signals in  
10 parallel and outputs the voltage to the drain buses 42-1  
to 42-N in parallel. By contrast, since the display  
section 30 of this embodiment of FIG. 1 has a  
constitution that the voltage corresponding to the  
signals 202-1 to 202-N input from the signal conversion  
15 section 20 is supplied to the drain buses 42-1 to 42-N  
from the input circuits 32-1 to 32-N, the horizontal  
register circuit 54 need not be provided, nor clock  
signals supplied to the horizontal register circuit 54  
are unnecessary, so that power consumption can be more  
20 reduced.

1            Depending on an application where the image  
display apparatus of this embodiment is used, the image  
display apparatus may have a constitution that the  
signal conversion section 20 is omitted and signals  
5    200-1 to 200-N output from the imaging section 10 are  
directly input to the input circuits 32-1 to 32-N.

10           FIG. 4 shows an alternative embodiment of the  
image display apparatus according to the present  
invention.       This image display apparatus has a  
constitution obtained by providing a parallel-to-serial  
conversion section 56 in the image display apparatus of  
FIG. 1.    This parallel-to-serial conversion section 56  
converts the signals 202-1 to 202-N, which are output  
15    in parallel from the signal conversion section 20, to  
serial signals 204 and outputs them.    The section 56  
outputs the signal similar to that generated by the  
conventional signal conversion section 62 shown in  
FIG. 6.

20           Also in this embodiment, power consumption can  
be reduced similarly to the embodiment of FIG. 1.    It  
should be noted that the image display apparatus can be  
constituted by omitting the display section 30 of  
25    FIG. 4.    In this case, the number of outputs of the  
signal conversion section 20 is not restricted to the  
number of pixels of the display section 30 in the  
horizontal direction.

30           FIG. 5 shows an embodiment of a display  
apparatus according to the present invention.    In this  
display apparatus, the imaging section 10 of FIG. 1 is  
omitted and a serial-to-parallel conversion section 58

1 is provided. This serial-to-parallel conversion  
section 58 converts signals 206 serially input thereto  
to parallel signals 202-1 to 202-N and outputs them to  
the signal conversion section 20. Also in this  
5 embodiment, power consumption can be reduced similarly  
to the embodiment shown in FIG. 1.

The entire disclosure of Japanese patent  
application No. 10247/1999 filed on January 19, 1999  
10 including the specification, claims, accompanying  
drawings and abstract of the disclosure is incorporated  
herein by reference in its entirety.

While the present invention has been  
15 described with reference to the particular illustrative  
embodiments, it is not to be restricted by those  
embodiments. It is to be appreciated that those  
skilled in the art can change or modify the embodiments  
without departing from the scope and spirit of the  
20 present invention.

WHAT IS CLAIMED IS:

1           1. An image display apparatus comprising:  
          imaging       section       having       photoelectric  
conversion devices arranged in the form of a matrix,  
said imaging section sequentially outputting signals  
5 generated by said photoelectric conversion devices in  
parallel column by column of said matrix; and

          display     section     having     display     devices  
arranged in the form of a matrix, which displays an  
image represented by signals applied thereto at the time  
10 of application of driving pulses, said display section  
applying the signals output in parallel from said  
imaging section to said display devices column by column  
and supplying said driving pulses line by line in a  
predetermined order.

1           2. The image display apparatus according to  
claim 1, wherein said imaging section comprises a CCD  
imaging device or a MOS imaging device.

1           3. The image display apparatus according to  
claim 1, wherein said display section comprises a liquid  
crystal display.

1           4. An image display apparatus comprising:  
          imaging       section       having       photoelectric  
conversion devices arranged in the form of a matrix,  
said imaging section sequentially outputting signals  
5 generated by said photoelectric conversion devices in  
parallel column by column of said matrix;

          signal     conversion     section     for     performing     a  
processing for the signals output from said imaging

section in parallel column by column and outputting the  
10 processed signals in parallel; and

display section having display devices  
arranged in the form of a matrix, which display an image  
represented by signals applied thereto at the time of  
application of driving pulses, said display section  
15 applying the signals output in parallel from said signal  
conversion section to said display devices column by  
column and supplying said driving pulses line by line in  
a predetermined order.

1 5. The image display apparatus according to  
claim 4, wherein said imaging section comprises a CCD  
imaging device or a MOS imaging device.

1 6. The image display apparatus according to  
claim 4, wherein said display section comprises a  
liquid crystal display.

1 7. The image display apparatus according to  
claim 4, said apparatus further comprising:

parallel-to-serial conversion section for  
converting the signals output in parallel from said  
signal conversion section to serial signals.

1 8. An image display apparatus comprising:  
imaging section having photoelectric  
conversion devices arranged in the form of a matrix,  
said imaging section sequentially outputting signals  
5 generated by said photoelectric conversion devices in  
parallel column by column of said matrix;

signal conversion section for performing a  
processing for the signals output in parallel from said

10 imaging section column by column and outputting the  
processed signals in parallel; and

parallel-to-serial conversion section for  
converting the signals output in parallel from said  
signal conversion section to serial signals.

1 9. The image display apparatus according to  
claim 8, wherein said imaging section comprises a CCD  
imaging device or a MOS imaging device.

1 10. A display apparatus comprising:

serial-to-parallel conversion section for  
converting signals serially input thereto to parallel  
signals and outputting the signals; and

5 display section having display devices  
arranged in the form of a matrix, which display an image  
represented by signals applied thereto at the time of  
application of driving pulses, said display section  
applying the signals output in parallel from said  
10 serial-to-parallel conversion section to said display  
devices column by column and supplying said driving  
pulses line by line in a predetermined order.

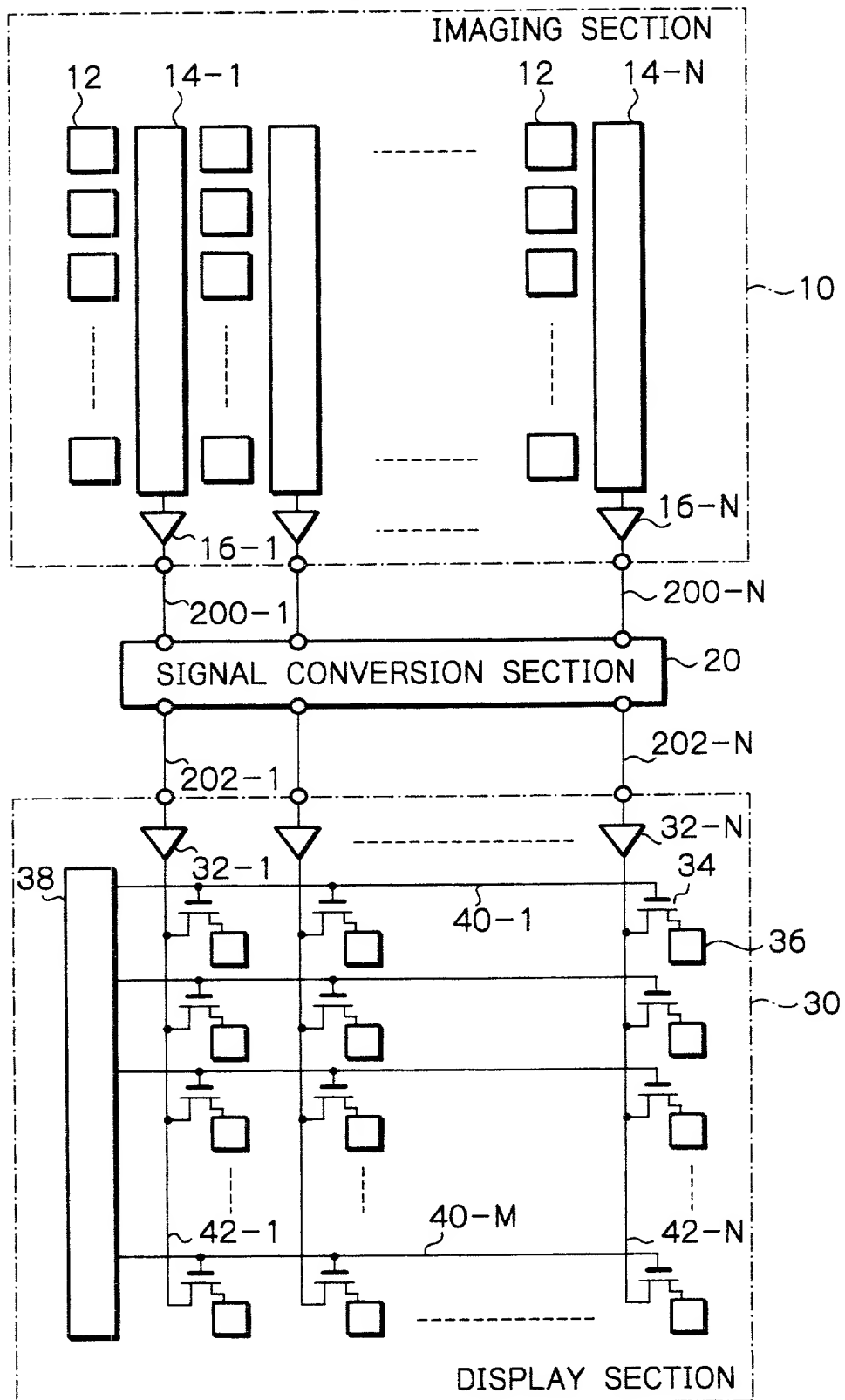
1 11. The display apparatus according to claim  
10, wherein said display section comprises a liquid  
crystal display.

ABSTRACT OF THE DISCLOSURE

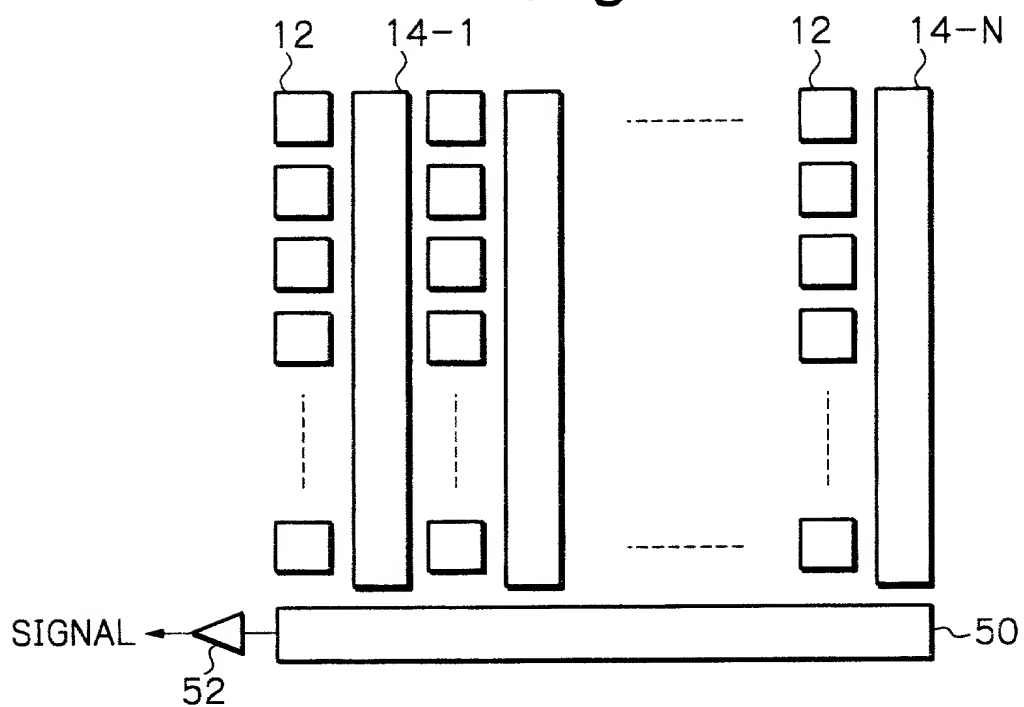
5 In an imaging section, an image of an object is converted to signal charge by photodiodes arranged in the form of a matrix, the signal charge is transferred to output circuits by vertical transfer paths, and then the signal charge transferred to the output circuits is converted to signal voltage by the output circuits. The signal voltage is output from the output circuits to a signal conversion section as signals. The signal conversion section performs a processing for the signals in parallel, and outputs the processed signals to a display section. In the display section, signals are converted to voltage by input circuits, and the voltage is respectively applied to drain buses. A vertical driving circuit scans gate buses, and supplies gate driving pulses. Field effect transistors supplied with the gate driving pulses store charge in response to the voltage applied to liquid crystal devices, thus displaying an image.



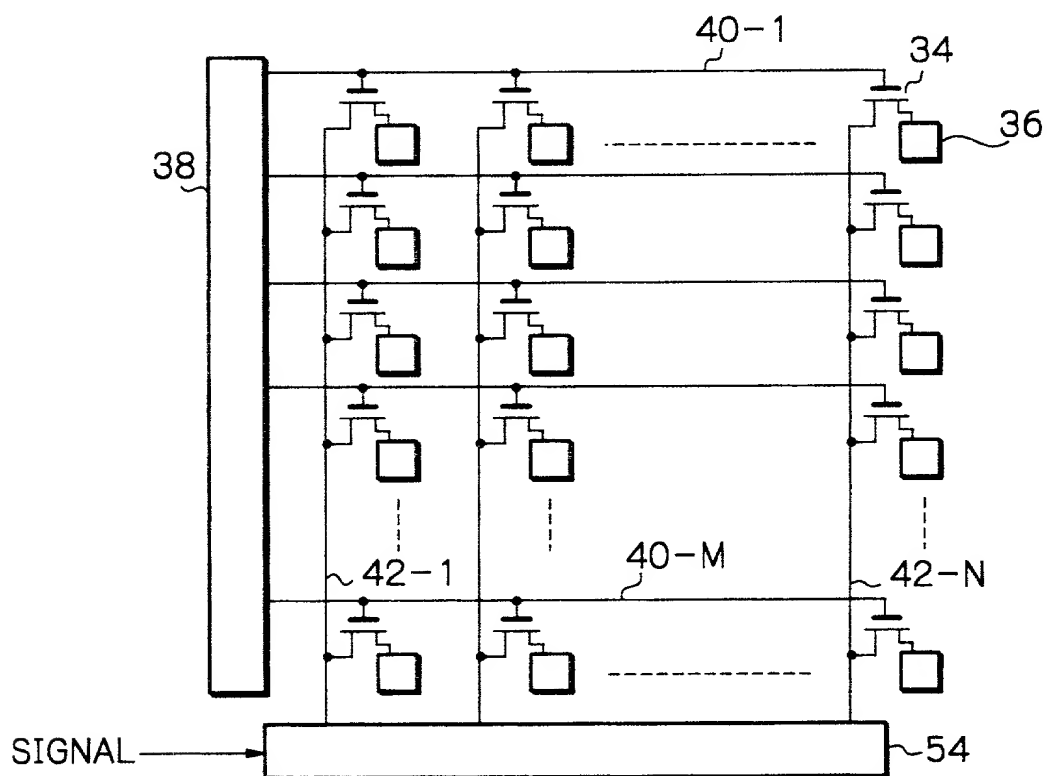
Fig. 1



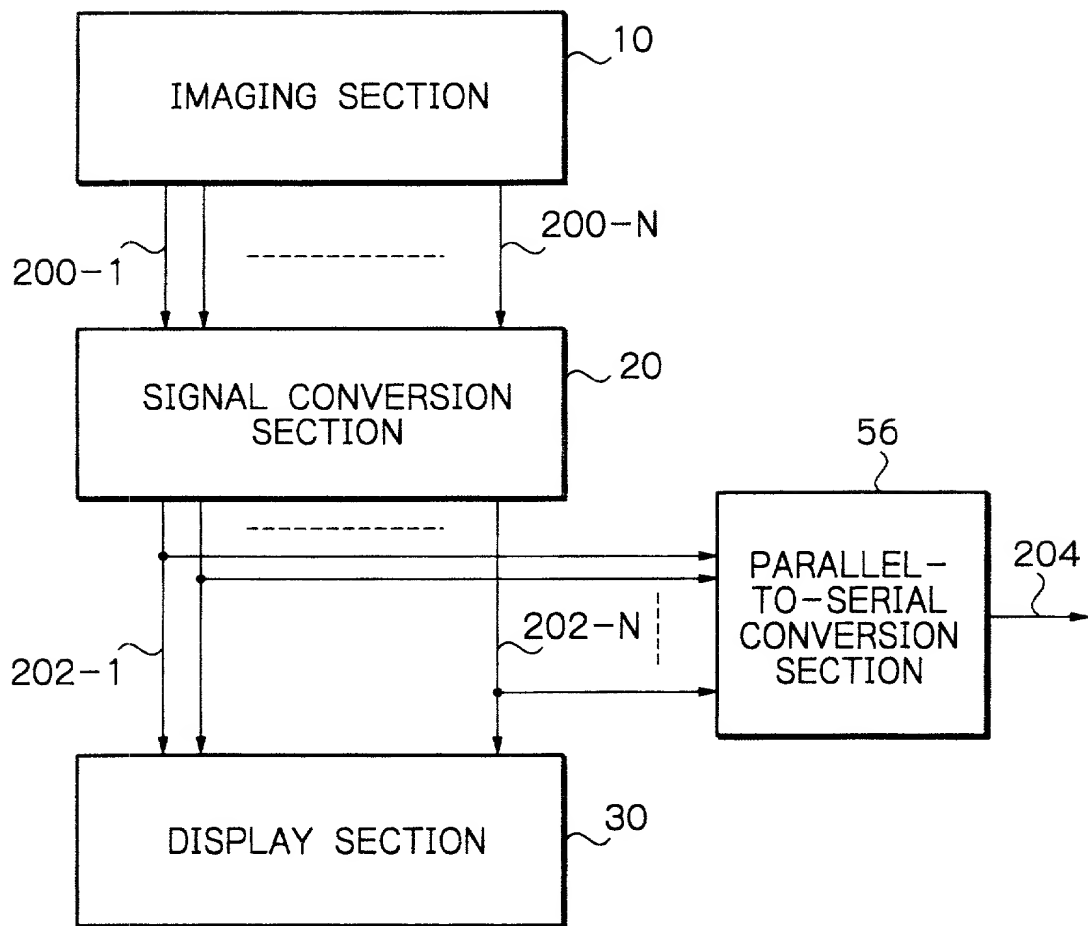
*Fig. 2*



*Fig. 3*



*Fig. 4*



*Fig. 5*

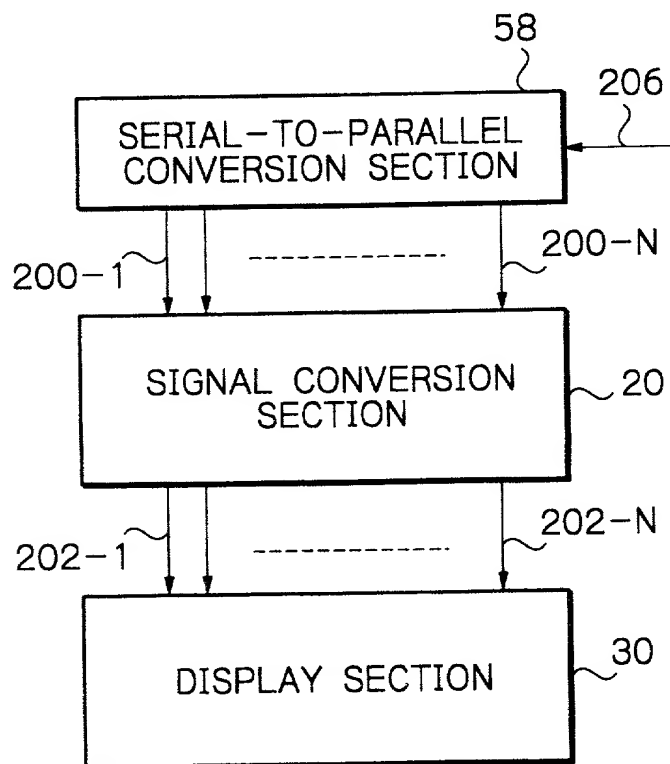
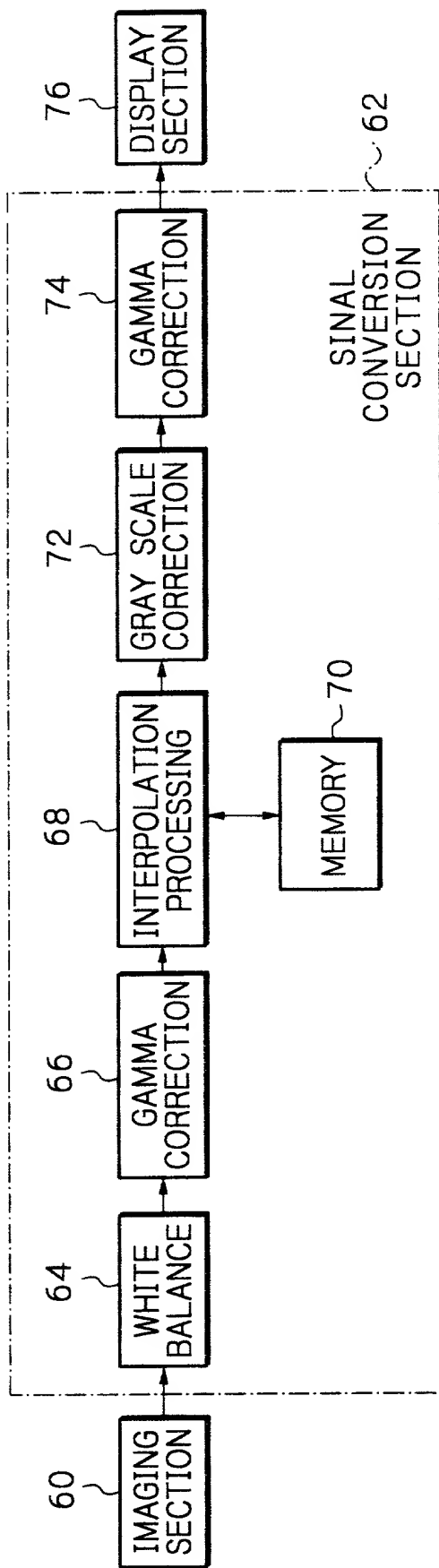


Fig. 6



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**COMBINED DECLARATION AND POWER OF ATTORNEY  
FOR PATENT AND DESIGN APPLICATIONS**

ATTORNEY DOCKET NO.

378-366P

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor (if only one inventor is named below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Insert Title:

**IMAGE DISPLAY APPARATUS FOR PHOTOGRAPHING AN OBJECT AND  
DISPLAYING THE PHOTOGRAPHED IMAGE**

Fill in Appropriate  
Information -  
For Use Without  
Specification  
Attached:

the specification of which is attached hereto. If not attached hereto,

the specification was filed on \_\_\_\_\_ as

United States Application Number \_\_\_\_\_; and /or

the specification was filed on \_\_\_\_\_ as PCT

International Application Number \_\_\_\_\_; and was

amended under PCT Article 19 on \_\_\_\_\_ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (six months for designs) prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 (a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Insert Priority  
Information:  
(if appropriate)

**Prior Foreign Application(s)**

10247/1999  
(Number)

Japan  
(Country)

January 19, 1999  
(Month/Day/Year Filed)

**Priority Claimed**

☒ Yes ☐ No

(Number)

(Country)

(Month/Day/Year Filed)

☐ Yes ☐ No

(Number)

(Country)

(Month/Day/Year Filed)

☐ Yes ☐ No

(Number)

(Country)

(Month/Day/Year Filed)

☐ Yes ☐ No

(Number)

(Country)

(Month/Day/Year Filed)

☐ Yes ☐ No

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below.

Insert Provisional  
Application(s):  
(if any)

(Application Number)

(Filing Date)

(Application Number)

(Filing Date)

**All Foreign Applications, if any, for any Patent or Inventor's Certificate Filed More Than 12 Months (6 Months for Designs) Prior To The Filing Date of This Application:**

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Information:  
(if appropriate)

Country

Application No

Date of Filing (Month/Day/Year)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Insert Prior U.S.  
Application(s):  
(if any)

(Application Number)

(Filing Date)

(Status - patented, pending, abandoned)

(Application Number)

(Filing Date)

(Status - patented, pending, abandoned)

I hereby appoint the following attorneys to prosecute this application and/or an international application based on this application and to transact all business in the Patent and Trademark Office connected therewith and in connection with the resulting patent based on instructions received from the entity who first sent the application papers to the attorneys identified below, unless the inventor(s) or assignee provides said attorneys with a written notice to the contrary:

Terrell C. Birch	(Reg. No. 19,382)	Raymond C. Stewart	(Reg. No. 21,066)
Joseph A. Kolasch	(Reg. No. 22,463)	James M. Slattery	(Reg. No. 28,380)
Bernard L. Sweeney	(Reg. No. 24,448)	Michael K. Mutter	(Reg. No. 29,680)
Charles Gorenstein	(Reg. No. 29,271)	Gerald M. Murphy, Jr.	(Reg. No. 28,977)
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Andrew D. Meikle	(Reg. No. 32,868)	Marc S. Weiner	(Reg. No. 32,181)
Joe McKinney Muncy	(Reg. No. 32,334)	<del>Andrew F. Reich</del>	<del>(Reg. No. 33,113)</del>
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Send Correspondence to:

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YOU MUST  
COMPLETE THE  
FOLLOWING:

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of First or Sole  
Inventor:  
Insert Name of Inventor  
Insert Date This  
Document is Signed  
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Insert Citizenship  
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Address  
Full Name of Second  
Inventor, if any:  
see above  
Full Name of Third  
Inventor, if any:  
see above  
Full Name of Fourth  
Inventor, if any:  
see above  
Full Name of Fifth  
Inventor, if any:  
see above

GIVEN NAME	FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
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Residence (City, State & Country)		CITIZENSHIP	
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POST OFFICE ADDRESS (Complete Street Address including City, State & Country)			
c/o Fuji Photo Film Co., Ltd., 11-46, Senzui 3-chome, Asaka-shi, Saitama, Japan			
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Residence (City, State & Country)		CITIZENSHIP	
POST OFFICE ADDRESS (Complete Street Address including City, State & Country)			
GIVEN NAME	FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
Residence (City, State & Country)		CITIZENSHIP	
POST OFFICE ADDRESS (Complete Street Address including City, State & Country)			
GIVEN NAME	FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
Residence (City, State & Country)		CITIZENSHIP	
POST OFFICE ADDRESS (Complete Street Address including City, State & Country)			
GIVEN NAME	FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
Residence (City, State & Country)		CITIZENSHIP	
POST OFFICE ADDRESS (Complete Street Address including City, State & Country)			